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ELECTRONIC DEVICE

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[There are no amendments to this patent.]

Abstract

Objective

To improve the manufacturing ease and the packing density in an electronic device in which IC chips such as LSI chips are assembled.

Constitution

Several IC chips 10 and 20 are fixed with several connecting bodies in an oppositely arranged state, while setting electrode forming surfaces inside, and are electrically connected. At the same time, electrical terminals such as lead 32 connected to an integrated circuit of at least one of the IC chips 10 and 20 are led to the outside from the space between the chips. Each connecting body consists of protruded electrodes 16 and 26, electrode connecting part 36, etc. Protruded electrodes 16, 17, 26, 27, etc., can be simply bonded in a face-to-face state by installing them in advance at the chips or leads. Also, a high-density packing is enabled by superposing and adhering several chip sets 50 with such a constitution.

Claims

1. An electronic device characterized by the fact that it is equipped with (a) a first integrated circuit chip in which a first integrated circuit and several electrodes of the circuit

are formed on one principal plane, (b) a second integrated circuit chip arranged in an opposite and adjoining state to one principal plane of the first integrated circuit chip and formed on one principal plane opposite to one principal plane of the above-mentioned first integrated circuit, and in which several electrodes of the circuit are formed in accordance with several electrodes of the above-mentioned first integrated circuit; (c) several connecting bodies interposed and arranged between two integrated circuit chips so that the above-mentioned first and second integrated circuit chips are fixed in the above-mentioned opposite and adjoining state, and that the corresponding electrodes of two integrated circuit chips are respectively electrically connected; and (d) several electric terminals that are electrically connected to at least one of the above-mentioned first and second integrated circuits between the above-mentioned first and second integrated circuit chips and led to the outside from two integrated circuit chips.

2. An electronic device characterized by the fact that it is equipped with (a) a first integrated circuit chip in which a first integrated circuit and several electrodes of the circuit are formed on one principal plane; (b) a second integrated circuit chip arranged in an opposite and adjoining state to one principal plane of the first integrated circuit chip and formed on one principal plane opposite to one principal plane of the above-mentioned first integrated circuit, and in which several electrodes of the circuit are formed in accordance with several electrodes of the above-mentioned first integrated circuit, (c) several connecting bodies interposed and arranged between two integrated circuit chips so that the above-mentioned first and second integrated circuit chips are fixed in the above-mentioned

opposite and adjoining state, and that the corresponding electrodes of two integrated circuit chips are respectively electrically connected, (d) several electric terminals that are electrically connected to at least one of the above-mentioned first and second integrated circuits between the above-mentioned first and second integrated circuit chips and led to the outside from two integrated circuit chips; and (e) a sealing body interposed and arranged between two integrated circuit chips so that part or all of each said first and second integrated circuit is airtightly sealed between the above-mentioned first and second integrated circuit chips.

3. An electronic device characterized by the fact that it is equipped with several chip sets consisting of (a) a first integrated circuit chip in which a first integrated circuit and several electrodes of the circuit are formed on one principal plane; (b) a second integrated circuit chip arranged in an opposite and adjoining state to one principal plane of the first integrated circuit, chip and formed on one principal plane opposite to one principal plane of the above-mentioned first integrated circuit and in which several electrodes of the circuit are formed in accordance with several electrodes of the above-mentioned first integrated circuit; (c) several connecting bodies interposed and arranged between two integrated circuit chips so that the above-mentioned first and second integrated circuit chips are fixed in the above-mentioned opposite and adjoining state, and that the corresponding electrodes of two integrated circuit chips are respectively electrically connected, and (d) several electric terminals electrically connected to at least one of the above-mentioned first and second integrated circuits between the above-mentioned first and second integrated circuit

chips and led to the outside from two integrated circuit chips; and that these chip sets are superposed and adhered on the principal plane opposite to the principal plane on which the above-mentioned electrodes are formed.

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